ABSTRACT

[0027] A system and method for testing the random access memory of a computer system is disclosed. A memory-testing engine is embedded in the utility bus controller of an application specific integrated circuit, which is coupled to a random access memory in need of testing. Upon receiving an initiation signal over a bus from the central processing unit, the memory-testing engine begins writing data to a targeted area of the memory, and then reading back the stored data and comparing the data to what was sent. Having the memory-testing engine distributed to the memory's being tested allows several memory devices to be tested simultaneously.